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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WERNER, BRIAN P	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/515,348	SPENCE, CHRISTOPHER A.	
	Examiner	Art Unit	
	Brian P. Werner	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-20 and 22-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-20 and 22-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the claim amendment and remarks received on January 10, 2005. Claims 1, 4-20 and 22-27 are now pending.

Information Disclosure Statement

2. The information disclosure statement filed on September 14,2004 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. While the IDS states that a form 1449 is "attached", no corresponding 1449 (i.e., the list of references for the examiner to initial as considered) is present in the file. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered. Submission of a form 1449 for submission of the references is suggested.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim Construction:

The term "figure of merit" is construed as a parameter relating to the measurement of a physical feature or features. In the context of the claimed inventions, the parameter relates to measuring semiconductor features. For example, claim 5 defines the term as a "line width", and claim 6 defines it as a "percentage difference". However, claims 5 and 6 are dependent claims, and according to the doctrine of claim differentiation, the term "figure of merit" as recited in the independent claims is broader than either of line width and percentage difference.

The term "critical dimensions" is construed as dimension of features that are critical to the operation of the semiconductor device.

4. Claims 1, 4-8, 10, 11, 13-15, 17-20 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Chang et al. (US 6,757,645 B2) and Fiekowsky (US 6,263,292 B1). Regarding claims 1, 4 and 27, Chang discloses a method for analyzing dimensional variations (figure 9), comprising: imaging a portion of a mask used in the wafer structure formation process (figure 9, numeral 915), the mask being formed by a mask manufacturing process (the "physical mask" 905 is inherently manufactured by a mask

manufacturing process – mask's don't spontaneously generate; e.g., see "mask manufacture) 705 in figure 7(a)); simulating lithographic processing using data received from or derived from the imaging of the portion of the mask (figure 9, numeral 950), thereby obtaining a simulated wafer structure (figure 9, numeral 970); simulating lithographic processing using mask design data corresponding to the imaged portion of the mask as an input (figure 9, numeral 960), thereby obtaining a second simulated wafer structure (figure 9, numeral 975); and comparing the first and second simulated wafer structures (figure 9, numeral 980). Note: Chang's defect analyzer 990 also comparison comprises "displaying the images 970 and 975, and displaying the differences between the two such that an operator can visually detect any differences" at column 21, line 14. While Chang does disclose a comparison of simulated wafer images as described above, Chang does not disclose a "user-selected figure of merit" for purposes of comparing the images. Fiekowsky discloses a mask inspection system (figure 1; "mask" at column 10, line 58), comprising providing a user with an option of selecting a figure of merit by which critical dimension variations between the images are to be calculated ("identifying and measuring a variety of features such as defects and line widths" at column 11, line 30; "user region of interest" at column 11, line 42; "the operator is able to enter review mode and to quickly surround spot 71 with a rough user region of interest 72 indicating the region that the user wishes to analyze and measure" at column 11, lines 47-50; Fiekowsky's figures of merit, e.g. as depicted at figures 3, are selected by the user depending upon what features the user chooses to examine based on the "region of interest" designated by the user; Further, Fiekowsky's figures of merit are used to measure "critical" dimensions – that is, dimension such as line width and height of features that may be deemed defects and thus critical to the operation of the semiconductor

device). It would have been obvious at the time the invention was made to one of ordinary skill in the art to add to the Chang "defect analyzer" (figure 9, numeral 990), a user selected figure of merit (e.g., "line widths ... heights" at column 4, Fiekowsky lines 21-22; "diameters" at Fiekowsky column 3, line 64) as taught by Fiekowsky, in order to provide the operator of Chang with "a measurement tool that provides an objective, practical and fast method for accurate sizing of mask features found with an automatic inspection tool" (Fiekowsky, column 3, lines 61-64). That is, the operator of Change would be provided with the ability to measure the "differences" between the two simulated mask patterns (e.g., as depicted by Chang at figures 17 and 20) using various figures of merit, in order to assess the relevancy and importance of those differences. Regarding claims 4 and 5 specifically, Fiekowsky as part of the Chang and Fiekowsky combination above further discloses performing actual calculations based on the user selected figure of merit (e.g., "line width dimension may be calculated" at column 16, line 66). Regarding claim 6, percentage of a difference area is one of many measures of differences between features that is well known, and would have been obvious to one of ordinary skill in the art in order to determine the extent of the difference. Regarding claim 17, Chang discloses transforming data of a first type, obtained in the imaging, to data of a second type, used in simulating (figure 9, numeral 930 transforms the acquired image data into defect area image information). Regarding claim 7, the same simulation method is used (figure 9, numerals 960 and 950 simulate using the same method, using the same lithography conditions at numerals 965). Regarding claims 8, 18, 19 and 20, aerial image simulation is disclosed (the "Hopkins model" is used at column 12, line 55, and it is an aerial simulation; i.e., see "Fast Aerial Image Computation" at column 13, line 30. Regarding claim 24, Chang overlays the simulated wafer

structures on a display screen (comprises "displaying the images 970 and 975, and displaying the differences between the two such that an operator can visually detect any differences" at column 21, line 14; see figures 17 and 20). Regarding claim 22, a comparison is disclosed as discussed above (i.e., figure 9, numeral 980). Regarding claims 10, 11 and 23, the simulated wafer structure is displayed ("displaying the images 970 and 975" at column 21, line 13). Regarding claim 11, overlapping images are displayed (figure 20, numeral 2030). Regarding claims 13-15, a SEM is used to generated the image as applied to claim 1 ("scanning electron microscope" at column 10, numeral 12). Regarding claim 26, the Chang determines and displays all dimensional variations between the simulated images as depicted in figures 17 and 20 (and "all" variations includes the "greatest" variation as claimed). Regarding claim 25, Chang anticipates comparing the two simulated wafer structures to ideal wafer structure (figure 20, mask image simulation 2020 and design data simulation 2050 are displayed, their difference is displayed at 2030, and the original design data is displayed at 2040. Given these windows of image information, Chang anticipates that an operator will look at all of them in his/her evaluation of the differences.

5. Claims 1, 4, 8, 9, 13-20 and 27, are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Fiekowsky (US 6,263,292 B1). Regarding claims 1, 4 and 27, Pierrat discloses a method of analyzing a wafer manufacturing process ("semiconductor devices ... detecting defects introduced during the photolithography process" at column 1, lines 5-7; "wafers" at column 1, line 18) comprising: imaging a portion of a mask used in the wafer structure formation process (figure 1, numeral 130 and figure 3,

numeral 230), the mask being formed by a mask manufacturing process (figure 3, numeral 220); simulating lithographic processing using data received from or derived from the imaging of the portion of the mask, thereby obtaining a simulated wafer structure (figure 1, numeral 180 and figure 3, numeral 260); simulating lithographic processing using mask design data corresponding to the imaged portion of the mask as an input, thereby obtaining a second simulated wafer structure (figure 1, numeral 185 and figure 3, numeral 265); and comparing the first and second simulated wafer structures (figure 1, numeral 140 and figure 3, numeral 270; the simulated wafer structure at numeral 260 is compared with the "result" of a simulation using design data at numeral 265, where the design data represents the desired wafer structure). While Pierrat discloses a comparison of simulated wafer images as described above, Pierrat does not disclose a "user-selected figure of merit" for purposes of comparing the images. Fiekowsky discloses a mask inspection system (figure 1; "mask" at column 10, line 58), comprising providing a user with an option of selecting a figure of merit by which critical dimension variations between the images are to be calculated ("identifying and measuring a variety of features such as defects and line widths" at column 11, line 30; "user region of interest" at column 11, line 42; "the operator is able to enter review mode and to quickly surround spot 71 with a rough user region of interest 72 indicating the region that the user wishes to analyze and measure" at column 11, lines 47-50; Fiekowsky's figures of merit, e.g. as depicted at figures 3, are selected by the user depending upon what features the user chooses to examine based on the "region of interest" designated by the user; Further, Fiekowsky's figures of merit are used to measure "critical" features – that is, features that may be deemed defects and thus critical to the operation of the semiconductor device). It would have been obvious at the time the invention was made to one of ordinary skill

in the art to add to the Pierrat "defect detection" (figure 1, numeral 140 and figure 3, numeral 270), a user selected figure of merit (e.g., "line widths ... heights" at column 4, Fiekowsky lines 21-22; "diameters" at Fiekowsky column 3, line 64) as taught by Fiekowsky, in order to provide the operator of Pierrat with "a measurement tool that provides an objective, practical and fast method for accurate sizing of mask features found with an automatic inspection tool" (Fiekowsky, column 3, lines 61-64). That is, the operator of Pierrat would be provided with the ability to measure the "differences" between the two simulated mask patterns using various figures of merit, in order to assess the relevancy and importance of those differences. Regarding claim 8, the first and second simulations are aerial simulations (the Pierrat simulations are aerial simulations; e.g., an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; the "simulation program logic is written in the C programming language" at column 6, line 16). Regarding claim 9, a simulation step is applied to the imaged data (i.e., figure 3, numeral 240), where this step is not applied to the mask data (as depicted in figure 3). Thus, the overall simulation processes of the mask data and the imaged data are different. Regarding claim 13, a SEM is used to capture the mask image ("SEM" at column 5, line 6). Regarding claim 14, the SEM data is transformed into computer readable data (i.e., an electron image is transformed into the computer readable format required by the simulator; stated another way, a computer cannot manipulate an electron image direction, thus there must be some transformation of the electron image into a format required by the simulator). Regarding claims 15 and 16, image analysis ("analyzes" at column 6, line 6) and scaling ("pixel erosion" at column 8, line 67; such an erosion algorithm reduces the size of a feature by eroding it away) of the data are performed. Regarding claim 17, optical data is

transformed into numerical computer data as depicted in figure 1 (i.e., light from 110 is passed through mask 161 and converted by sensor 130 to computer readable data). Regarding dependent claim 18, an aerial image simulation program is disclosed (the Pierrat simulation is an aerial simulation; e.g., an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; the "simulation program logic is written in the C programming language" at column 6, line 16). Regarding dependent claim 19, the simulating includes simulating the developed resist image ("elevation data" at column 5, line 56 and "sidewalls" at column 6, line 5, both of which correspond to the "resist layer" at column 5, line 62, are simulated using "algorithms which emulate the behavior of resist material" at column 5, line 65). Regarding claim 20, the simulating uses an aerial image microscope system (an "aerial image measurement system" at column 5, line 8 is used to capture the mask image from which the aerial simulation is performed; given that the structures of the mask being captured by Pierrat are extremely small, one of ordinary skill would understand that the "aerial image measurement system" is a microscope system).

6. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Pierrat et al. (US 6,091,845 A) and Fiekowsky (US 6,263,292 B1) as applied to claim 1 above, and further in combination with Sheng (US 6,477,265 A). Pierrat discloses generating first and second simulated structures as described above, whereby the structures are aligned and compared for defects (figure 1, numeral 140 and figure 3, numeral 270). Regarding claims 10 and 11, Pierrat does not disclose displaying the first and second simulated structures on a display screen, at least partially overlapping one another. Sheng discloses a

photolithographic inspection system (Abstract, line 2), comprising the comparison of two image images to detect differences that are defects (figure 5; "defect detection" at column 3, line 56), wherein Sheng teaches displaying the first and second images on a display screen, at least partially overlapping one another ("image display 44 displays the superimposed image" at column 3, line 41). It would have been obvious at the time the invention was made to one of ordinary skill in the art to superimpose and display the first and second simulated images of Pierrat, as taught by Sheng, so that in fulfilling Pierrat's requirement for defect inspection, the images of Pierrat "can easily be inspected for defects" (Sheng, column 2, line 21, line 25, and column 3, line 61).

Response to Arguments

7. Applicant's arguments filed with the amendment have been fully considered but they are not persuasive. Applicant argues, at response page 7, that:

"While Fiekowsky deals with feature measurement, it lacks teaching of providing a user with an option of selecting a FOM by which critical dimension variations between first and second simulated structures are to be calculated. Further, Fiekowsky is silent with respect to critical dimension variations between the first and second simulated wafer structures being calculated based on the user-selected FOM."

In response, it is pointed out that Fiekowsky discloses:

1. Providing a user with an option of selecting a FOM (The "operator is able to enter review mode and to quickly surround spot 71 with a rough user region of interest 72 indicating the region that the user wishes to analyze and measure" at column 11, lines 47-50. Fiekowsky's figures of merit, e.g. as depicted at figures 3, are selected by the user depending upon what features the user chooses to examine based on the "region of interest" designated by the user).

2. The FOM by which critical dimension variations between first and second simulated structures are to be calculated (Fiekowsky's figures of merit are used to measure "critical" dimensions – that is, dimension such as line width and height of features that may be deemed defects and thus critical to the operation of the semiconductor device).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Werner whose telephone number is 571-272-7401. The examiner can normally be reached on M-F, 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh M. Mehta can be reached on 571-272-7453. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Werner
Primary Examiner
Art Unit 2621
May 27, 2005

BRIAN WERNER
PRIMARY EXAMINER